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(54) **ELECTRO-OPTIC MODULATOR DEVICE
AND METHOD OF MAKING THE SAME**

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(2013.01); **H01S 5/187** (2013.01)

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257/98, 437
See application file for complete search history.

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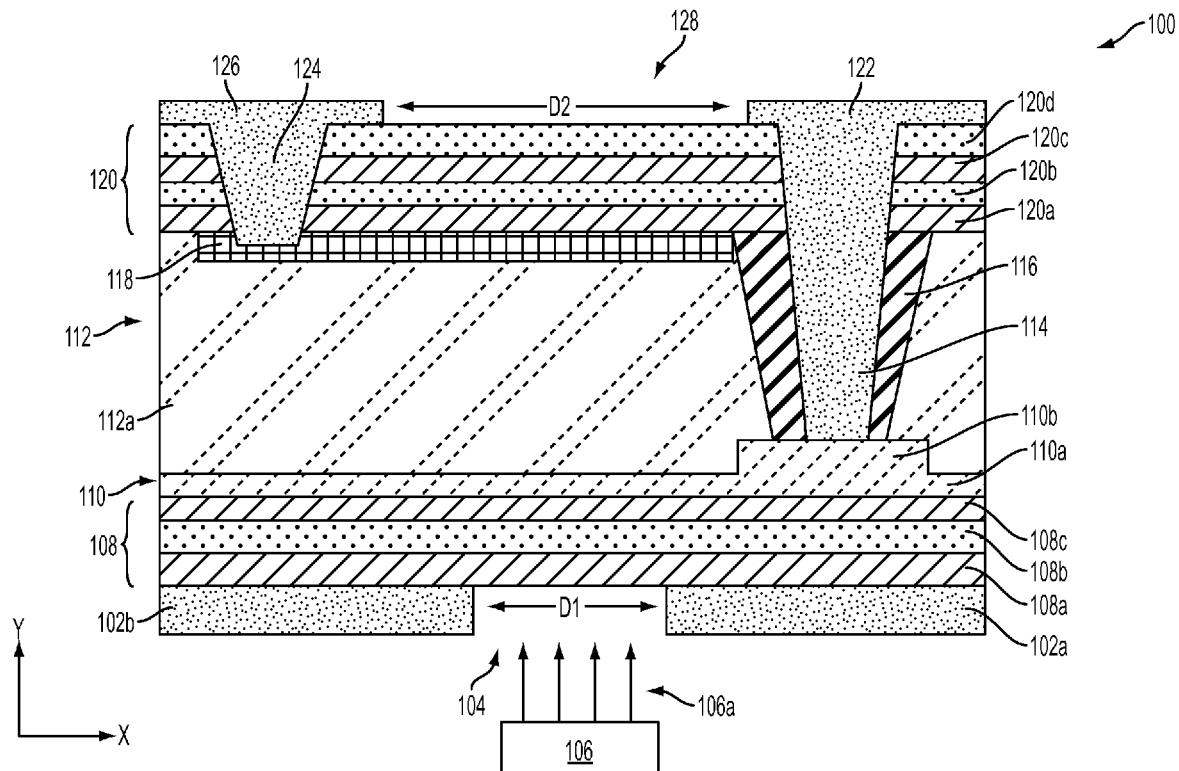
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(57) **ABSTRACT**

An electro-optic modulator including a semiconductor region, a first reflecting region over the semiconductor region and an anti-reflecting region on an opposite surface of the semiconductor region from the first reflecting layer. The semiconductor region includes a first doped region and a second doped region.

20 Claims, 4 Drawing Sheets



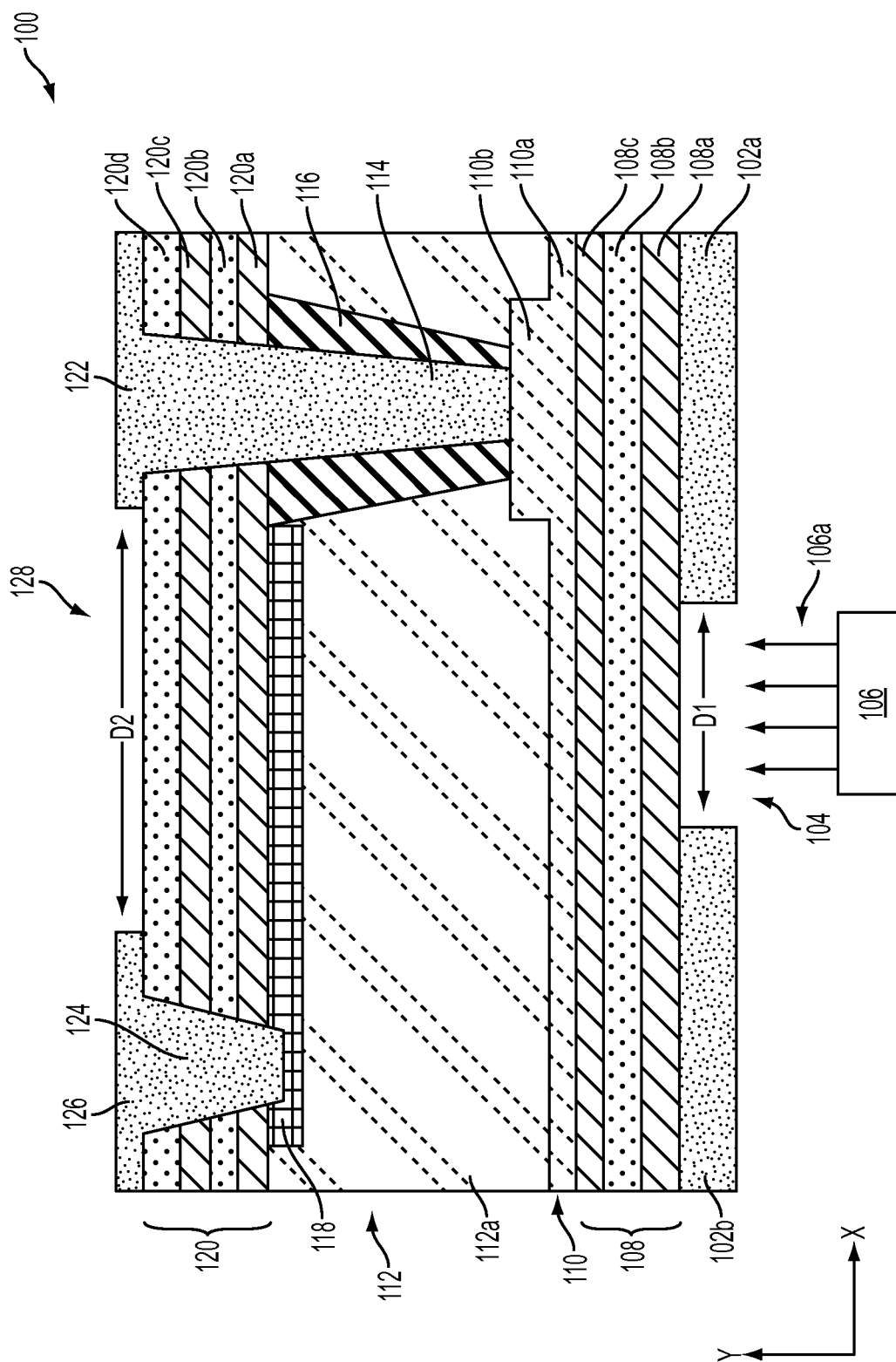


FIG. 1

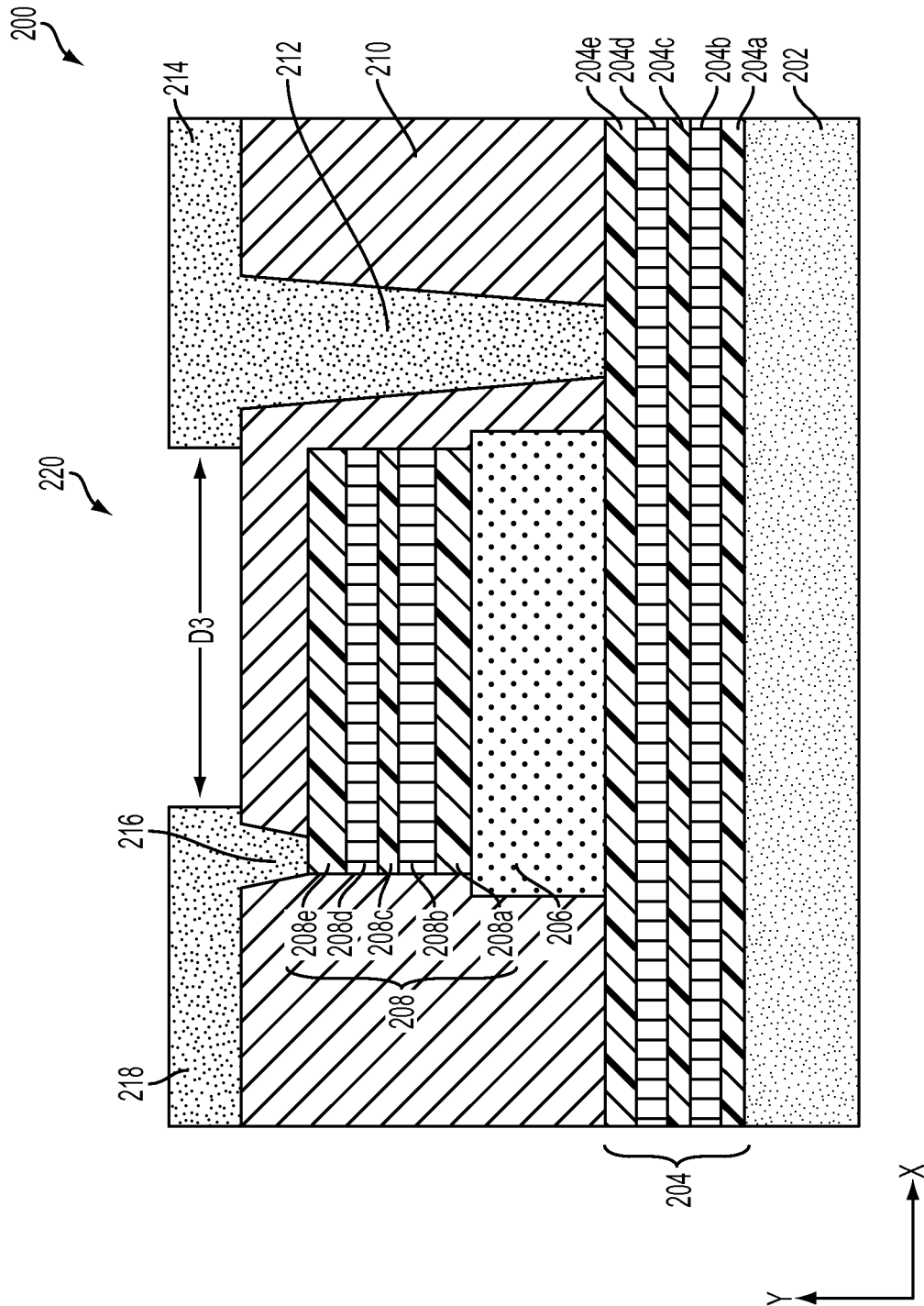
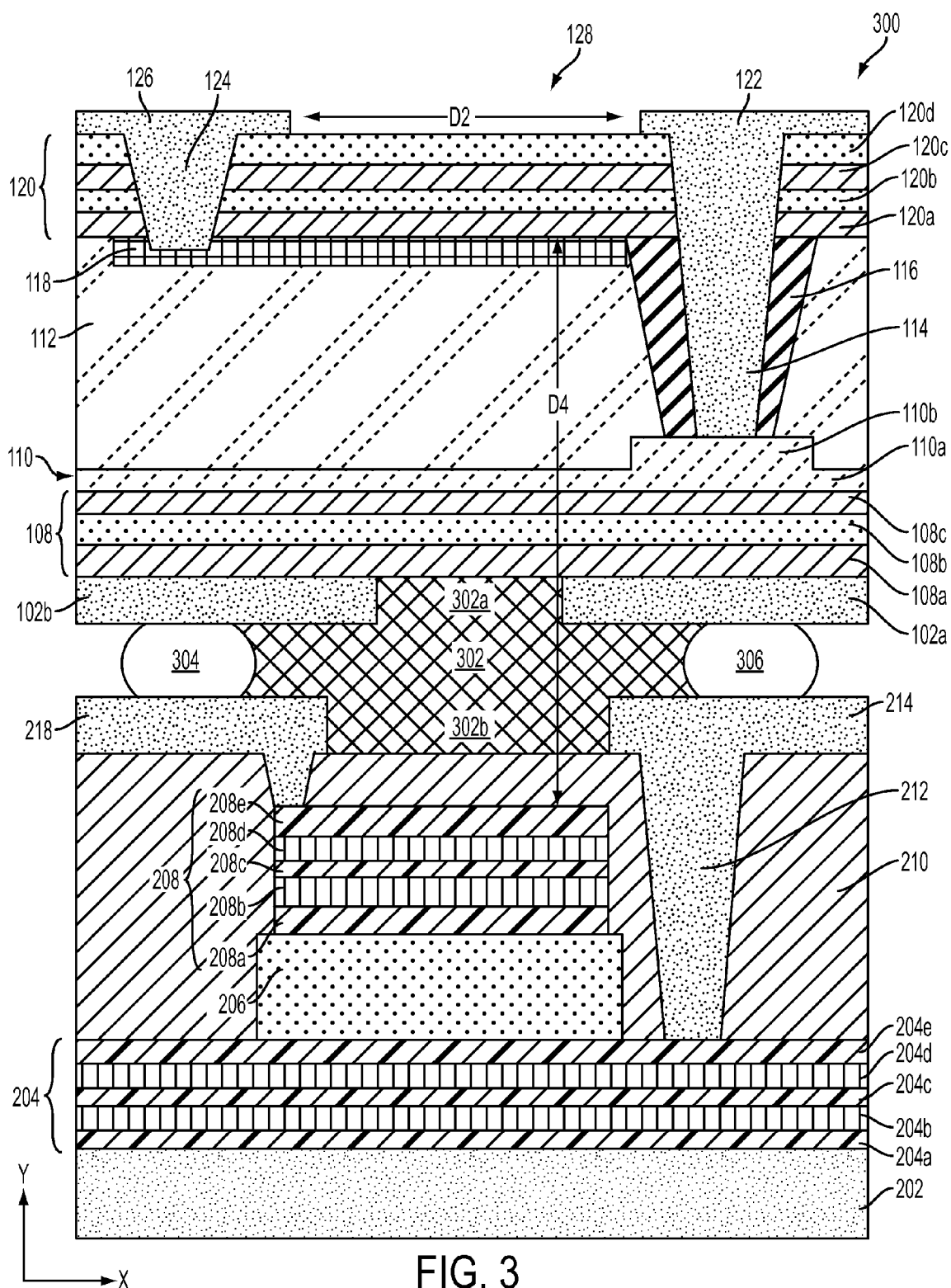


FIG. 2



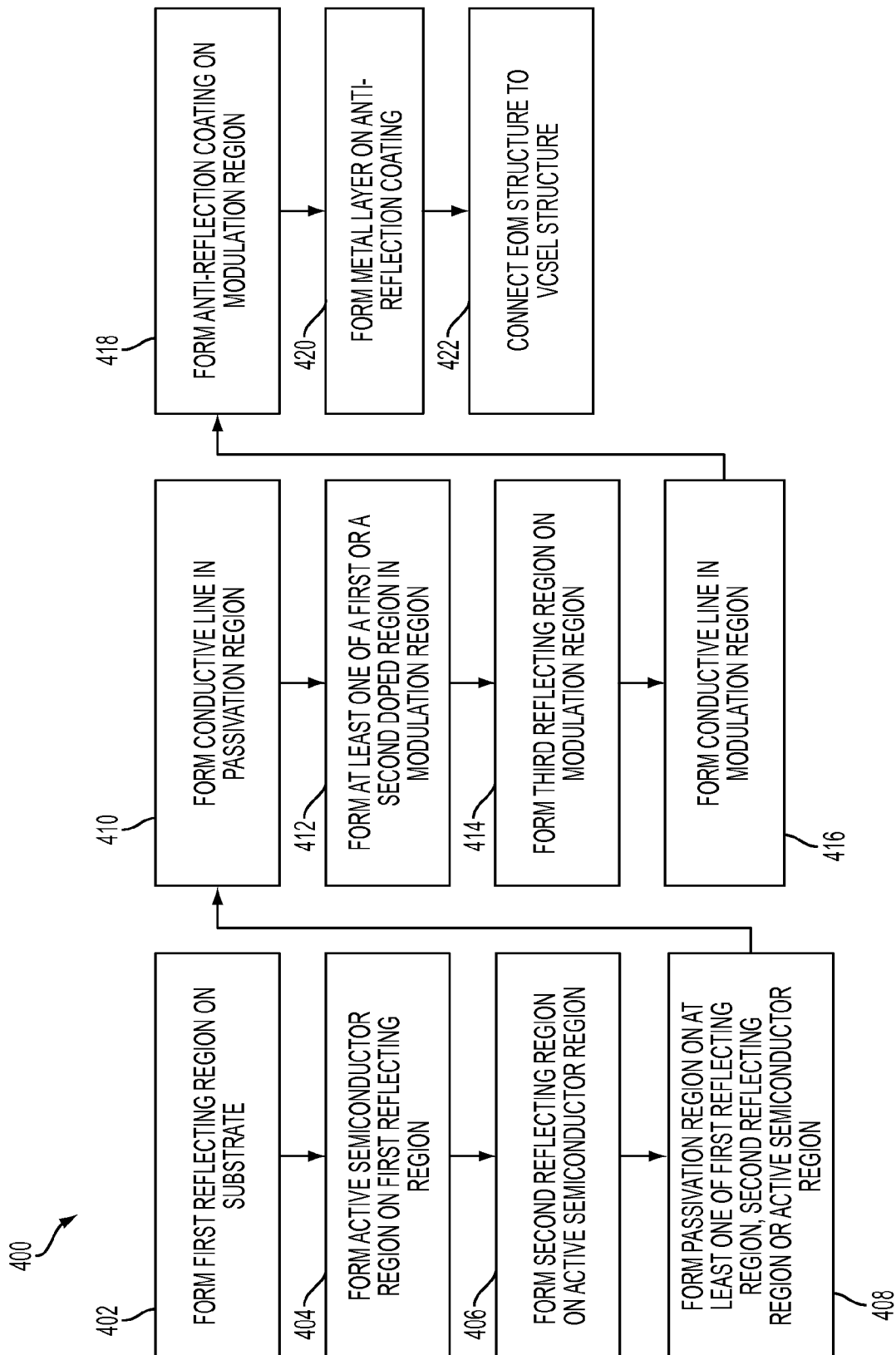


FIG. 4

ELECTRO-OPTIC MODULATOR DEVICE AND METHOD OF MAKING THE SAME

BACKGROUND

Optical signals are usable for various applications including high speed and secure data transmission between two devices. In some applications, a semiconductor device includes at least an integrated circuit (IC or “chip”) having an optical component. An electro-optic effect is a change in the optical properties of a material in response to an applied electric field that varies at a lower frequency when compared with the frequency of light. Modulation is the process of varying one or more properties of a periodic waveform, called a carrier signal, with a modulating signal. An electro-optic modulator (EOM) is an optical semiconductor device in which a signal-controlled element/material exhibiting the electro-optic effect is used to modulate a beam of light. The phase, frequency, amplitude, or polarization of the beam of light may be modulated.

BRIEF DESCRIPTION OF THE DRAWINGS

One or more embodiments are illustrated by way of example, and not by limitation, in the figures of the accompanying drawings, wherein elements having the same reference numeral designations represent like elements throughout. It is emphasized that, in accordance with standard practice in the industry various features may not be drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features in the drawings may be arbitrarily increased or reduced for clarity of discussion.

FIG. 1 is a cross sectional view of an Electro-Optic Modulator (EOM) structure in accordance with one or more embodiments;

FIG. 2 is a cross sectional view of a Vertical Cavity Surface Emitting Laser (VCSEL) structure in accordance with one or more embodiments;

FIG. 3 is a cross sectional view of an EOM/VCSEL structure in accordance with one or more embodiments; and

FIG. 4 is a flow chart of a method of making an EOM/VCSEL structure in accordance with one or more embodiments.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the disclosed subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are examples and are not intended to be limiting.

This description of the embodiments is intended to be read in connection with the accompanying drawings, which are to be considered part of the entire written description. In the description, relative terms such as “before,” “after,” “above,” “below,” “up,” “down,” “top” and “bottom” as well as derivative thereof (e.g., “horizontally,” “downwardly,” “upwardly,” etc.) should be construed to refer to the orientation as then described or as shown in the drawing under discussion. These relative terms are for convenience of description and do not require that the system be constructed or operated in a particular orientation. Terms concerning attachments, coupling and the like, such as “connected” and “interconnected,” refer to a relationship wherein components are attached to one another either directly or indirectly through intervening components, unless expressly described otherwise.

FIG. 1 is a cross-sectional view of an EOM structure 100 in accordance with one or more embodiments. EOM structure 100 comprises base conductive line 102a, base conductive line 102b, first opening 104, Anti-Reflective Coating (ARC) region 108, first doped region 110, modulation region 112, first conductive line 114, first passivation region 116, second doped region 118, first upper reflecting region 120, first conductive layer 122, second conductive line 124, second conductive layer 126 and second opening 128.

A base conductive line 102a and base conductive line 102b are adjacent to another and separated by a distance D1. The placement of the base conductive line 102a and base conductive line 102b forms the first opening 104 between each conductive line. The first opening 104 has a width of distance D1. In some embodiments, the distance D1 is a diameter of the first opening 104. In some embodiments, the first opening 104 is circular, rectangular, square, hexagonal, or other geometric shapes. In some embodiments, a distance D1 ranges from about 5 μm to about 20 μm .

In some embodiments, the base conductive line 102a and base conductive line 102b include more than one conductive portion. In some embodiments, base conductive line 102a or base conductive line 102b is in a two-dimensional plane. In some embodiments, base conductive line 102a and base conductive line 102b are three-dimensional structures. In some embodiments, the three-dimensional structure includes a combination of conductive lines on different layers of EOM structure 100. In some embodiments, base conductive line 102a or base conductive line 102b extend parallel to another. In some embodiments, base conductive line 102a or base conductive line 102b extends along an angled direction with respect to an x-axis and a y-axis of EOM structure 100.

In some embodiments, the base conductive line 102a and base conductive line 102b include a single port for either receiving or outputting an electrical current. In some embodiments, the base conductive line 102a and base conductive line 102b include more than one port and are each capable of both receiving and outputting an electrical current. In some embodiments, base conductive line 102a and base conductive line 102b include copper, aluminum, nickel, tungsten, titanium, or another suitable conductive material. In some embodiments, a thickness of base conductive line 102a ranges from about 500 nm to about 5 μm . In some embodiments, a thickness of base conductive line 102b ranges from about 500 nm to about 5 μm .

The first opening 104 receives electromagnetic radiation 106a from an electromagnetic radiation source 106. The electromagnetic radiation 106a includes a collimated signal. In some embodiments, a wavelength of the electromagnetic radiation 106a ranges from about 925 nanometers (nm) to about 2 μm . In some embodiments, the electromagnetic radiation 106a includes infrared light. In some embodiments, the electromagnetic radiation source 106 includes a III-V semiconductor material device. In some embodiments, the electromagnetic radiation source 106 includes a III-V semiconductor Vertical Cavity Surface Emitted Laser (VCSEL). In some embodiments, EOM structure 100 is configured to receive an infrared signal with a diameter ranging from about 5 μm to about 20 μm . In some embodiments, EOM structure 100 is configured to receive an infrared signal with an optical power ranging from about 100 nW to about 20 mW.

ARC region 108 is over base conductive line 102a, base conductive line 102b and first opening 104. ARC region 108 includes layers of materials, e.g., ARC layers 108a, 108b and 108c, having corresponding refractive indices, e.g., n_{108a} , n_{108b} , n_{108c} , to reduce the reflection of incident electromagnetic radiation 106a, thereby improving the efficiency of the

EOM structure **100**. ARC region **108** includes ARC layers **108a**, **108b** and **108c**. In some embodiments, ARC region **108** includes one or more ARC layers. ARC layer **108c** is over ARC layer **108b** and ARC layer **108a**. ARC layer **108b** is over ARC layer **108a**. ARC layer **108a** is over base conductive line **102a**, base conductive line **102b** and first opening **104**.

In some embodiments, ARC region **108** is positioned in a two-dimensional plane which is parallel to the base conductive line **102a** and base conductive line **102b**. In some embodiments, ARC region **108** is a three-dimensional structure over base conductive line **102a** and base conductive line **102b**. In some embodiments, each ARC layer **108a**, **108b** and **108c** is positioned in a two-dimensional plane which is parallel to each ARC layer **108a**, **108b** and **108c**.

In some embodiments, ARC region **108** comprises a stack of alternating layers of anti-reflecting materials, e.g., ARC layers **108a**, **108b** and **108c**, with alternating high and low refractive indices. In some embodiments, ARC layers **108a** and **108c** are the same material and the corresponding indices of refraction, n_{108a} and n_{108c} , are equal. In some embodiments, ARC layer **108a** is a different material from ARC layer **108b**, and the corresponding indices of refraction, n_{108a} and n_{108b} , are not equal. In some embodiments, ARC layer **108c** is a different material from ARC layer **108b**, and the corresponding indices of refraction, n_{108c} and n_{108b} , are not equal.

In some embodiments, ARC **108** region reflects about 3% of all incident radiation waves. In some embodiments, the number of ARC layers ranges from about 3 layers to about 10 layers. In some embodiments, ARC region **108** reduces chaotic oscillation/resonance of the incident electromagnetic radiation **106a** from the ARC **108**/base conductive line **102a**, base conductive line **102b** and first opening **104** interface. In some embodiments, the thickness of each ARC layer **108a**, **108b** and **108c** ranges from about 230 nm to about 500 nm.

In some embodiments, the index of refraction (n_{108a}) for the ARC layer **108a** ranges from about 1.6 to about 2.8. In some embodiments, the index of refraction (n_{108b}) for the ARC layer **108b** ranges from about 1.3 to about 2.0. In some embodiments, the index of refraction (n_{108c}) for the ARC layer **108c** ranges from about 1.6 to about 2.8. In some embodiments, one or more of ARC reflecting layer **108a** or ARC reflecting layer **108c** includes a dielectric material comprising SiO_2 , low-k dielectrics; any other suitable material; or combinations thereof. In some embodiments, ARC reflecting layer **108b** includes a dielectric material comprising SiN; SiON; high-k dielectrics; any other suitable material; or combinations thereof. In some embodiments, ARC reflecting region **108** includes a dielectric material including SiO_2 ; SiN; SiON; low-k dielectrics; high-k dielectrics; any other suitable material; or combinations thereof. In some embodiments, the ARC region **108** is formed by CVD, ALD, or other processes. In some embodiments, the ARC region **108** has a multilayer structure and is formed in a multiple-step process. In some embodiments, the thickness of each ARC reflecting layer **108a**, **108b** and **108c** ranges from about 60 nm to about 400 nm. In some embodiments, the thickness of ARC region **108** ranges from about 60 nm to about 400 nm.

Modulation region **112** is over ARC region **108**. Modulation region **112** includes a semiconductor region **112a** between a first doped region **110** of the semiconductor region and a second doped region **118** of the semiconductor region. In some embodiments, modulation region **112** is positioned in a two-dimensional plane which is parallel to the ARC region **108**. In some embodiments, modulation region **112** is a three-dimensional structure over ARC region **108**. In some embodiments, first doped region **110** is adjacent to the modulation region **112** and ARC region **108** interface. In some embodi-

ments, second doped region **118** is adjacent to the modulation region **112** and first upper reflecting region **120** interface.

In some embodiments, modulation region **112** includes a P-I-N junction, where the P-region and N-region include first doped region **110** and the second doped region **118**, and the I-region includes a lightly doped near-intrinsic semiconductor region **112a**. In some embodiments, the semiconductor region **112a** includes a bulk material or a quantum well. In some embodiments, the quantum well includes a single quantum well. In some embodiments, the quantum well includes a multiple quantum well including multiple quantum well layers. In some embodiments, the bulk material includes an elemental semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure, an alloy semiconductor including SiGe; any other suitable material; or combinations thereof. In some embodiments, the multiple quantum well includes alternating layers of $\text{Si}_x\text{Ge}_{1-y}/\text{Si}_y\text{Ge}_{1-x}$, where $0 \leq x$ and $y \leq 1$. In some embodiments, the number of quantum well layers ranges from about 1 layer to about 31 layers. In some embodiments, the thickness of the modulation region **112** is less than or about equal to 2 μm . In some embodiments, semiconductor region **112a** includes an elementary semiconductor including silicon or germanium in crystal, polycrystalline, or an amorphous structure, an alloy semiconductor including SiGe; any other suitable material; or combinations thereof. In some embodiments, the modulation region **112** is formed by backside illuminated processes, KOH backside etch processes with an implantation etch stop; or other suitable processes. In some embodiments, the modulation region **112** is formed in a multiple-step process.

First doped region **110** is over the ARC region **108**. First doped region **110** includes a lower first doped region **110a** and an upper first doped region **110b**. In some embodiments, first doped region **110** is positioned in a two-dimensional plane which is parallel to the ARC region **108**. In some embodiments, first doped region **110** is a three-dimensional structure over ARC region **108**. In some embodiments, lower first doped region **110a** is positioned in a two-dimensional plane which is parallel to the ARC region **108**. In some embodiments, lower first doped region **110a** is a three-dimensional structure over ARC region **108**. In some embodiments, lower first doped region **110a** is positioned along the modulation region **112**/ARC region **108** interface. In some embodiments, upper first doped region **110b** is electrically connected to first conductive line **114**. In some embodiments, the upper first doped region **110b** is a doped contact implant.

Second doped region **118** is over the first doped region **110** and the ARC region **108**. In some embodiments, second doped region **118** is positioned in a two-dimensional plane which is parallel to the ARC region **108**. In some embodiments, second doped region **118** is a three-dimensional structure over ARC region **108**. In some embodiments, second doped region **118** is positioned adjacent an interface formed by the modulation region **112** and first upper reflecting region **120**.

In some embodiments, first doped region **110** or second doped region **118** are doped with dopants utilized for Silicon, Silicon/Germanium and Germanium. In some embodiments, first doped region **110** is doped with an n-type material, including Phosphorous or Arsenic, or any other suitable material, and second doped region **118** is doped with a p-type material, including Boron, or any other suitable material. In some embodiments, first doped region **110** is doped with a p-type material, including Boron, or any other suitable material, and second doped region **118** is doped with an n-type material, including Phosphorous or Arsenic, or any other suitable material. In some embodiments, the thickness of the

first doped region **110** ranges from about 30 nm to about 300 nm. In some embodiments, the thickness of the second doped region **118** ranges from about 30 nm to about 300 nm. In some embodiments, the dopant concentration of the first doped region **110** ranges from about 10^{17} ions/cm³ to about 10^{20} ions/cm³. In some embodiments, the dopant concentration of the second doped region **118** ranges from about 10^{17} ions/cm³ to about 10^{20} ions/cm³.

First upper reflecting region **120** is over the modulation region **112**. First upper reflecting region **120** includes layers of materials, e.g., first upper reflecting layers **120a**, **120b**, **120c** and **120d**, having corresponding refractive indices, e.g., n_{120a} , n_{120b} , n_{120c} and n_{120d} , in order to reflect incident electromagnetic radiation **106a**, and improving the efficiency of the EOM structure **100**. In some embodiments, first upper reflecting region **120** is a distributed Bragg reflector, which uses alternating layers of materials having different refractive indices to reflect emitted light from modulation region **112**.

First upper reflecting region **120** includes first upper reflecting layers **120a**, **120b**, **120c** and **120d**. In some embodiments, first upper reflecting region **120** includes one or more reflecting layers. First upper reflecting layer **120d** is over first upper reflecting layer **120c**, first upper reflecting layer **120b** and first upper reflecting layer **120a**. First upper reflecting layer **120c** is over first upper reflecting layer **120b** and first upper reflecting layer **120a**. First upper reflecting layer **120b** is over first upper reflecting layer **120a**. First upper reflecting layer **120a** is over modulation region **112**.

In some embodiments, first upper reflecting region **120** is positioned in a two-dimensional plane which is parallel to the modulation region **112**. In some embodiments, first upper reflecting region **120** is a three-dimensional structure over modulation region **112**. In some embodiments, each first upper reflecting layer **120a**, **120b**, **120c** and **120d** is positioned in a two-dimensional plane which is parallel to each first upper reflecting layer **120a**, **120b**, **120c** and **120d**.

In some embodiments, first upper reflecting region **120** comprises a stack of alternating layers of reflecting materials, e.g., first upper reflecting layers **120a**, **120b**, **120c** and **120d**, with alternating high and low refractive indices. In some embodiments, first upper reflecting layers **120a** and **120c** are the same material and the corresponding indices of refraction, n_{120a} and n_{120c} , are equal. In some embodiments, first upper reflecting layers **120b** and **120d** are the same material, and the corresponding indices of refraction, n_{120b} and n_{120d} , are equal. In some embodiments, first upper reflecting layer **120a** is a different material from first upper reflecting layer **120b**, and the corresponding indices of refraction, n_{120a} and n_{120b} , are not equal. In some embodiments, first upper reflecting layer **120c** is a different material from first upper reflecting layer **120b**, and the corresponding indices of refraction, n_{120a} and n_{120b} , are not equal. In some embodiments, first upper reflecting layer **120c** is a different material from first upper reflecting layer **120d**, and the corresponding indices of refraction, n_{120c} and n_{120d} , are not equal.

In some embodiments, the index of refraction, n_{120a} , for the first upper reflecting layer **120a** ranges from about 2.0 to about 3.4. In some embodiments, the index of refraction, n_{120b} , for the first upper reflecting layer **120b** ranges from about 1.3 to about 1.6. In some embodiments, the index of refraction, n_{120c} , for the first upper reflecting layer **120c** ranges from about 2.0 to about 3.4. In some embodiments, the index of refraction, n_{120d} , for the first upper reflecting layer **120d** ranges from about 1.3 to about 1.6.

In some embodiments, the first upper reflecting layer **120a** includes a dielectric material with a high refractive index including SiNx (where $x < 1$); AN; Si; high-k dielectric; any

other suitable material; or combinations thereof. In some embodiments, the first upper reflecting layer **120b** includes a dielectric material with a low refractive index including SiO₂; low-k dielectric; any other suitable material; or combinations thereof. In some embodiments, the first upper reflecting layer **120c** includes a dielectric material with a high refractive index including SiNx (where $x < 1$); AN; Si; high-k dielectric; any other suitable material; or combinations thereof. In some embodiments, the first upper reflecting layer **120d** includes a dielectric material with a low refractive index including SiO₂; low-k dielectric; any other suitable material; or combinations thereof.

In some embodiments, the first upper reflecting region **120** is formed by chemical vapor deposition (CVD), atomic layer deposition (ALD), or other processes. In some embodiments, the first upper reflecting region **120** is formed without the use of III-V epitaxial layers. In some embodiments, the first upper reflecting region **120** has a multilayer structure and is formed in a multiple-step process. In some embodiments, the number of first upper reflecting layers ranges from about 10 layers to about 20 layers. In some embodiments, the thickness of each first upper reflecting layer **120a**, **120b**, **120c** and **120d** ranges from about 60 nm to about 400 nm.

First conductive line **114** extends through first upper reflecting region **120** and partially through modulation region **112**. First conductive line **114** is used to electrically connect first conductive layer **122** to first doped region **110**. In some embodiments, first conductive line **114** is a metal line, a via, a through silicon via (TSV), an inter-level via (ILV), or another suitable conductive line. In some embodiments, first conductive line **114** includes copper, aluminum, nickel, titanium, tungsten or another suitable conductive material. In some embodiments, first conductive line **114** is a same material as first conductive layer **122**. In some embodiments, first conductive line **114** is a different material from first conductive layer **122**. In some embodiments, first conductive line **114** includes one or more conductive line portions. In some embodiments, first conductive line **114** is in first doped region **110**.

First conductive layer **122** is over first upper reflecting region **120** and is used to electrically connect to the first doped region **110** by the first conductive line **114**. In some embodiments, the first conductive layer **122** includes more than one conductive portion. In some embodiments, first conductive layer **122** is in a two-dimensional plane. In some embodiments, first conductive layer **122** is a three-dimensional structure. In some embodiments, the three-dimensional structure includes a combination of conductive lines on different layers of EOM structure **100**. In some embodiments, first conductive layer **122** extends parallel to first upper reflecting region **120**. In some embodiments, first conductive layer **122** extends along an angled direction with respect to an x-axis and a y-axis of EOM structure **100**.

In some embodiments, first conductive layer **122** includes a single port for either receiving or outputting an electrical current. In some embodiments, first conductive layer **122** includes more than one port and is capable of both receiving and outputting an electrical current. In some embodiments, first conductive layer **122** includes copper, aluminum, nickel, tungsten, titanium, or another suitable conductive material. In some embodiments, a thickness of the first conductive layer **122** ranges from about 0.5 μ m to about 5 μ m.

First passivation region **116** extends circumferentially around the outer surface of first conductive line **114**. First passivation region **116** electrically isolates the first conductive line **114** from the second doped region **118**. First passivation region **116** electrically isolates the first doped region

110 from the second doped region 118. In some embodiments, the first passivation region 116 includes a dielectric material including SiO₂ or SiN; any other suitable material; or combinations thereof. In some embodiments, the first passivation region 116 is formed by CVD, or other processes. In some embodiments, a thickness of the first passivation region 116 ranges from about 100 nm to about 3,000 nm.

Second conductive line 124 extends through first upper reflecting region 120 and partially through modulation region 112. Second conductive line 124 is used to electrically connect second conductive layer 126 to second doped region 118. In some embodiments, second conductive line 124 is a metal line, a via, a through silicon via (TSV), an inter-level via (ILV), or another suitable conductive line. In some embodiments, second conductive line 124 includes copper, aluminum, nickel, titanium, tungsten or another suitable conductive material. In some embodiments, second conductive line 124 is a same material as second conductive layer 126. In some embodiments, second conductive line 124 is a different material from second conductive layer 126. In some embodiments, second conductive line 124 includes one or more conductive line portions. In some embodiments, second conductive line 124 is in second doped region 118.

Second conductive layer 126 is over first upper reflecting region 120 and is used to electrically connect to the second doped region 118 by the second conductive line 124. In some embodiments, the second conductive layer 126 includes more than one conductive portion. In some embodiments, second conductive layer 126 is in a two-dimensional plane. In some embodiments, second conductive layer 126 is a three-dimensional structure. In some embodiments, the three-dimensional structure includes a combination of conductive lines on different layers of EOM structure 100. In some embodiments, second conductive layer 126 extends parallel to first upper reflecting region 120. In some embodiments, second conductive layer 126 extends along an angled direction with respect to an x-axis and a y-axis of EOM structure 100.

In some embodiments, second conductive layer 126 includes a single port for either receiving or outputting an electrical current. In some embodiments, second conductive layer 126 includes more than one port and is capable of both receiving and outputting an electrical current. In some embodiments, second conductive layer 126 includes copper, aluminum, nickel, tungsten, titanium, or another suitable conductive material. In some embodiments, a thickness of the second conductive layer 126 ranges from about 0.5 μm to about 5 μm .

A first conductive layer 122 and second conductive layer 126 are adjacent to another and separated by a distance D2. The placement of the first conductive layer 122 and second conductive layer 126 forms the second opening 128 between each conductive layer. The second opening 128 has a width of distance D2. In some embodiments, the distance D2 is a diameter of the second opening 128. In some embodiments, the second opening 128 is circular, rectangular, square, hexagonal, or other geometric shapes. In some embodiments, a distance D2 ranges from about 10 μm to about 20 μm . In some embodiments, the ratio of the distance D1:D2 ranges from about 1:3, 1:2.5, 1:2, 1:1.5, 1:1, 1.5:1, 2:1, 2.5:1 or 3:1.

In some embodiments, first conductive layer 122 and second conductive layer 126 are configured to receive a modulated input bias signal which ranges from about 0 to 1.5 volts for a quantum well semiconductor region 112a. In some embodiments, first conductive layer 122 and second conductive layer 126 are configured to receive a modulated input bias signal which ranges from about 0 to 5.0 volts for a bulk material semiconductor region 112a. In some embodiments,

the modulated received input bias signal controls the refraction index of the modulating region 112, which controls the amount of modulation performed by the EOM structure 100. In some embodiments, EOM structure 100 is configured to operate with a bandwidth of about 50 Gigahertz (GHz). In some embodiments, EOM structure 100 is configured to output a modulated signal with an intensity which ranges from about 0.2 milliwatts (mw) to about 5 mw. In some embodiments, EOM structure 100 is configured to output an infrared modulated signal with a diameter of about 20 μm or less. In some embodiments, EOM structure 100 is configured to output an infrared signal for use in a single-mode optical fiber. In some embodiments, EOM structure 100 is configured to output an infrared signal for use in a multi-mode optical fiber. In some embodiments, EOM structure 100 is configured to output an infrared modulated signal with a wavelength ranging from about 925 nm to about 2000 nm. In some embodiments, the EOM structure 100 is usable for optical communications. In some embodiments, EOM structure 100 is configured to output a modulated signal to contain data. In some embodiments, EOM structure 100 is configured to output a modulated signal that is tunable. In some embodiments, EOM structure 100 is configured to output an amplitude modulated signal. In some embodiments, EOM structure 100 is configured to output a frequency modulated signal. In some embodiments, EOM structure 100 is configured to output a phase modulated signal. In some embodiments, EOM structure 100 is configured to output a polarization modulated signal.

FIG. 2 is a cross-sectional view of a VCSEL structure 200 in accordance with one or more embodiments. VCSEL structure 200 is an embodiment of electromagnetic radiation source 106 shown in FIG. 1. VCSEL structure 200 comprises substrate 202, first lower reflecting region 204, active semiconductor region 206, second upper reflecting region 208, second passivation layer 210, third conductive line 212, third conductive layer 214, fourth conductive line 216, fourth conductive layer 218 and third opening 220.

In some embodiments, substrate 202 includes a compound semiconductor including gallium arsenic or indium phosphide; any other suitable material; or combinations thereof. In some embodiments, a thickness of the substrate 202 ranges from about 3 μm to about 350 μm . In some embodiments, the substrate 202 has a multilayer structure. In some embodiments, substrate 202 includes a III-V semiconductor combination.

First lower reflecting region 204 is over the substrate 202. First lower reflecting region 204 includes layers of materials, e.g., first lower reflecting layers 204a, 204b, 204c, 204d and 204e, having corresponding refractive indices, e.g., n_{204a} , n_{204b} , n_{204c} , n_{204d} and n_{204e} , in order to reflect incident electromagnetic radiation. In some embodiments, first lower reflecting region 204 is a distributed Bragg reflector, which uses alternating layers of materials having different refractive indices to reflect emitted light from active semiconductor region 206.

First lower reflecting region 204 includes first lower reflecting layers 204a, 204b, 204c, 204d and 204e. In some embodiments, first lower reflecting region 204 includes one or more reflecting layers. First lower reflecting layer 204e is over first lower reflecting layer 204d, first lower reflecting layer 204c, first lower reflecting layer 204b and first lower reflecting layer 204a. First lower reflecting layer 204d is over first lower reflecting layer 204c, first lower reflecting layer 204b and first lower reflecting layer 204a. First lower reflecting layer 204c is over first lower reflecting layer 204b and first lower reflecting layer 204a. First lower reflecting layer 204b

is over first lower reflecting layer **204a**. First lower reflecting layer **204a** is over substrate **202**.

In some embodiments, first lower reflecting region **204** is positioned in a two-dimensional plane which is parallel to the substrate **202**. In some embodiments, first lower reflecting region **204** is a three-dimensional structure over substrate **202**. In some embodiments, each first lower reflecting layer **204a**, **204b**, **204c**, **204d** and **204e** is positioned in a two-dimensional plane which is parallel to each first lower reflecting layer **204a**, **204b**, **204c**, **204d** and **204e**.

In some embodiments, first lower reflecting region **204** comprises a stack of alternating layers of reflecting materials, e.g., first lower reflecting layers **204a**, **204b**, **204c**, **204d** and **204e**, with alternating higher and lower refractive indices. In some embodiments, first lower reflecting layers **204a**, **204c** and **204e** are the same material and the corresponding indices of refraction, n_{204a} , n_{204c} and n_{204e} , are equal. In some embodiments, first lower reflecting layers **204b** and **204d** are the same material and the corresponding indices of refraction, n_{204b} and n_{204d} , are equal.

In some embodiments, first lower reflecting layer **204a** is a different material from first lower reflecting layer **204b**, and the corresponding indices of refraction, n_{204a} and n_{204b} , are not equal. In some embodiments, first lower reflecting layer **204c** is a different material from first lower reflecting layer **204b**, and the corresponding indices of refraction, n_{204c} and n_{204b} , are not equal. In some embodiments, first lower reflecting layer **204c** is a different material from first lower reflecting layer **204d**, and the corresponding indices of refraction, n_{204c} and n_{204d} , are not equal. In some embodiments, first lower reflecting layer **204d** is a different material from first lower reflecting layer **204e**, and the corresponding indices of refraction, n_{204d} and n_{204e} , are not equal.

In some embodiments, the first lower reflecting layer **204a** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, the first lower reflecting layer **204b** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, the first lower reflecting layer **204c** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, the first lower reflecting layer **204d** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, the first lower reflecting layer **204e** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, when additional reflecting layers are added to the first lower reflecting region **204**, the additional layers include InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof.

In some embodiments, the first lower reflecting region **204** is formed by CVD, ALD, or other processes. In some embodiments, the first lower reflecting region **204** has a multilayer structure and is formed in a multiple-step process. In some embodiments, the number of first lower reflecting layers ranges from about 10 layers to about 20 layers. In some embodiments, the thickness of each first lower reflecting layer **204a**, **204b**, **204c**, **204d** and **204e** ranges from about 60 nm to about 200 nm.

Active semiconductor region **206** is over first lower reflecting region **204**. In some embodiments, active semiconductor region **206** is positioned in a two-dimensional plane which is

parallel to the first lower reflecting region **204**. In some embodiments, active semiconductor region **206** is a three-dimensional structure over first lower reflecting region **204**. In some embodiments, the active semiconductor region **206** includes layers of InGaAsP or AlGaInAs; any other suitable material; or combinations thereof. In some embodiments, the active semiconductor region **206** includes one or more quantum well layers. In some embodiments, each quantum well layer includes InGaAsP, AlGaInAs; any other suitable material; or combinations thereof. In some embodiments, active semiconductor region **206** includes a multiple quantum well where multiple well layers, e.g., InGaAsP and AlGaInAs, are positioned in an alternating pattern. In some embodiments, the thickness of the active semiconductor region **206** ranges from about 3 nm to about 12 nm. In some embodiments, active semiconductor region **206** includes layers of III-V materials which, when in use, emit infrared light.

Second upper reflecting region **208** is over the active semiconductor region **206**. Second upper reflecting region **208** includes layers of materials, e.g., second upper reflecting layers **208a**, **208b**, **208c**, **208d** and **208e**, having corresponding refractive indices, e.g., n_{208a} , n_{208b} , n_{208c} , n_{208d} and n_{208e} , in order to reflect incident electromagnetic radiation. In some embodiments, second upper reflecting region **208** is a distributed Bragg reflector, which uses alternating layers of materials having different refractive indices to reflect emitted light from active semiconductor region **206**.

Second upper reflecting region **208** includes second upper reflecting layers **208a**, **208b**, **208c**, **208d** and **208e**. In some embodiments, second upper reflecting region **208** includes one or more reflecting layers. Second upper reflecting layer **208e** is over second upper reflecting layer **208d**, second upper reflecting layer **208c**, second upper reflecting layer **208b** and second upper reflecting layer **208a**. Second upper reflecting layer **208d** is over second upper reflecting layer **208c**, second upper reflecting layer **208b** and second upper reflecting layer **208a**. Second upper reflecting layer **208c** is over second upper reflecting layer **208b** and second upper reflecting layer **208a**. Second upper reflecting layer **208b** is over second upper reflecting layer **208a**. Second upper reflecting layer **208a** is over active semiconductor region **206**.

In some embodiments, second upper reflecting region **208** is positioned in a two-dimensional plane which is parallel to the active semiconductor region **206**. In some embodiments, second upper reflecting region **208** is a three-dimensional structure over active semiconductor region **206**. In some embodiments, each second upper reflecting layer **208a**, **208b**, **208c**, **208d** and **208e** is positioned in a two-dimensional plane which is parallel to each second upper reflecting layer **208a**, **208b**, **208c**, **208d** and **208e**.

In some embodiments, second upper reflecting region **208** comprises a stack of alternating layers of reflecting materials, e.g., second upper reflecting layers **208a**, **208b**, **208c**, **208d** and **208e**, with alternating higher and lower refractive indices. In some embodiments, second upper reflecting layers **208a**, **208c** and **208e** are the same material and the corresponding indices of refraction, n_{208a} , n_{208c} and n_{208e} , are equal. In some embodiments, second upper reflecting layers **208b** and **208d** are the same material and the corresponding indices of refraction, n_{208b} and n_{208d} , are equal.

In some embodiments, second upper reflecting layer **208a** is a different material from second upper reflecting layer **208b**, and the corresponding indices of refraction, n_{208a} and n_{208b} , are not equal. In some embodiments, second upper reflecting layer **208c** is a different material from second upper reflecting layer **208b**, and the corresponding indices of refraction, n_{208c} and n_{208b} , are not equal. In some embodiments,

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second upper reflecting layer **208c** is a different material from second upper reflecting layer **208d**, and the corresponding indices of refraction, n_{208c} and n_{208d} , are not equal. In some embodiments, second upper reflecting layer **208d** is a different material from second upper reflecting layer **208e**, and the corresponding indices of refraction, n_{208d} and n_{208e} , are not equal.

In some embodiments, the second upper reflecting layer **208a** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, the second upper reflecting layer **208b** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, the second upper reflecting layer **208c** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, the second upper reflecting layer **208d** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, the second upper reflecting layer **208e** includes InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof. In some embodiments, when additional reflecting layers are added to the second upper reflecting region **208**, the additional layers include InGaAsP—InP, AlAs—AlGaAs, AlGaInAs—AlInAs, AlGaAsSb—AlAsSb; any other suitable material; or combinations thereof.

In some embodiments, the second upper reflecting region **208** is formed by CVD, ALD, or other processes. In some embodiments, the second upper reflecting region **208** has a multilayer structure and is formed in a multiple-step process. In some embodiments, the number of second upper reflecting layers ranges from about 5 layers to about 15 layers. In some embodiments, the thickness of each second upper reflecting layer **208a**, **208b**, **208c**, **208d** and **208e** ranges from about 60 nm to about 200 nm.

Second passivation region **210** is over first lower reflecting region **204**, active semiconductor region **206** and second upper reflecting region **208**. Second passivation region **210** extends circumferentially around the outer surface of third conductive line **212** or fourth conductive line **216**. Second passivation region **210** electrically isolates the third conductive line **212** from the second upper reflecting region **208**. Second passivation region **210** electrically isolates the fourth conductive line **216** from the first lower reflecting region **204**. Second passivation region **210** electrically isolates the first lower reflecting region **204** from the second upper reflecting region **208**. In some embodiments, the second passivation region **210** includes a dielectric material with a high refractive index including SiNx (where $x < 1$); any other suitable material; or combinations thereof. In some embodiments, the second passivation region **210** includes a dielectric material with a low refractive index including SiO₂; low-k dielectric; any other suitable material; or combinations thereof. In some embodiments, the second passivation region **210** is formed by CVD, spin-on polymeric dielectric or other processes. In some embodiments, the second passivation region **210** ranges from about 3 μm to about 20 μm . In some embodiments, the second passivation region **210** includes one or more layers.

Third conductive line **212** extends through second passivation region **210**. Third conductive line **212** is used to electrically connect third conductive layer **214** to first lower reflecting region **204**. In some embodiments, third conductive line **212** is a metal line, a via, a through silicon via (TSV), an inter-level via (ILV), or another suitable conductive line. In

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some embodiments, third conductive line **212** includes copper, aluminum, nickel, titanium, tungsten or another suitable conductive material. In some embodiments, third conductive line **212** is a same material as third conductive layer **214**. In some embodiments, third conductive line **212** is a different material from third conductive layer **214**. In some embodiments, third conductive line **212** includes one or more conductive line portions.

Third conductive layer **214** is over second passivation region **210** and is used to electrically connect to the first lower reflecting region **204** by the third conductive line **212**. In some embodiments, the third conductive layer **214** includes more than one conductive portion. In some embodiments, third conductive layer **214** is in a two-dimensional plane. In some embodiments, third conductive layer **214** is a three-dimensional structure. In some embodiments, the three-dimensional structure includes a combination of conductive lines on different layers of VCSEL structure **200**. In some embodiments, third conductive layer **214** extends parallel to second passivation region **210**. In some embodiments, third conductive layer **214** extends along an angled direction with respect to an x-axis and a y-axis of VCSEL structure **200**.

In some embodiments, third conductive layer **214** includes a single port for either receiving or outputting an electrical current. In some embodiments, third conductive layer **214** includes more than one port and is capable of both receiving and outputting an electrical current. In some embodiments, third conductive layer **214** includes copper, aluminum, nickel, tungsten, titanium, or another suitable conductive material. In some embodiments, a thickness of the third conductive layer **214** ranges from about 0.2 μm to about 5 μm .

Fourth conductive line **216** partially extends through second passivation region **210**. Fourth conductive line **216** is used to electrically connect fourth conductive layer **218** to second upper reflecting region **208**. In some embodiments, fourth conductive line **216** is a metal line, a via, a through silicon via (TSV), an inter-level via (ILV), or another suitable conductive line. In some embodiments, fourth conductive line **216** includes copper, aluminum, nickel, titanium, tungsten or another suitable conductive material. In some embodiments, fourth conductive line **216** is a same material as fourth conductive layer **218**. In some embodiments, fourth conductive line **216** is a different material from fourth conductive layer **218**. In some embodiments, fourth conductive line **216** includes one or more conductive line portions.

Fourth conductive layer **218** is over second passivation region **210** and is used to electrically connect to the second upper reflecting region **208** by the fourth conductive line **216**. In some embodiments, the fourth conductive layer **218** includes more than one conductive portion. In some embodiments, fourth conductive layer **218** is in a two-dimensional plane. In some embodiments, fourth conductive layer **218** is a three-dimensional structure. In some embodiments, the three-dimensional structure includes a combination of conductive lines on different layers of VCSEL structure **200**. In some embodiments, fourth conductive layer **218** extends parallel to second passivation region **210**. In some embodiments, fourth conductive layer **218** extends along an angled direction with respect to an x-axis and a y-axis of VCSEL structure **200**.

In some embodiments, fourth conductive layer **218** includes a single port for either receiving or outputting an electrical current. In some embodiments, fourth conductive layer **218** includes more than one port and is capable of both receiving and outputting an electrical current. In some embodiments, fourth conductive layer **218** includes copper, aluminum, nickel, tungsten, titanium, or another suitable con-

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ductive material. In some embodiments, a thickness of the fourth conductive layer **218** ranges from about 0.2 μm to about 5 μm .

A third conductive layer **214** and fourth conductive layer **218** are placed adjacent to another and separated by a distance **D3**. The placement of the third conductive layer **214** and fourth conductive layer **218** forms a third opening **220** between each conductive layer. The third opening **220** has a width of distance **D3**. In some embodiments, the distance **D3** is a diameter of the third opening **220**. In some embodiments, the third opening **220** is circular, rectangular, square, hexagonal, or other geometric shapes. In some embodiments, a distance **D3** ranges from about 10 μm to about 15 μm . In some embodiments, third conductive layer **214** and fourth conductive layer **218** are configured to receive an input signal which controls the infrared laser output of VCSEL **200**.

In some embodiments, VCSEL structure **200** is a III-V vertical cavity laser with an output wavelength ranging from about 925 nm to about 2000 nm. In some embodiments, VCSEL structure **200** is an upwardly directed vertical cavity laser. In some embodiments, VCSEL structure **200** is a downwardly directed vertical cavity laser. In some embodiments, VCSEL structure **200** is configured to operate with a bandwidth of about 50 Gigahertz (GHz).

FIG. 3 is a cross-sectional view of an EOM/VCSEL structure **300** in accordance with one or more embodiments. EOM/VCSEL structure **300** includes an embodiment of EOM structure **100** shown in FIG. 1 with similar elements coupled to an embodiment of VCSEL structure **200** shown in FIG. 2 with similar elements. EOM/VCSEL structure **300** includes EOM structure **100**, VCSEL structure **200**, insulating region **302**, first connector portion **304** and second connector portion **306**. The EOM structure **100** and VCSEL structure **200** are placed adjacent to another. The top surface of the second upper reflecting region **208** is separated a distance **D4** from the top surface of the modulation region **112**. In some embodiments, the distance **D4** is about 25 μm or less. In some embodiments, EOM structure **100** is bonded to the VCSEL structure **200** using a laser bonding process, a conductive adhesive layer, soldering process or another suitable bonding process.

First connector portion **304** is over fourth conductive layer **218** and is used to connect the EOM structure **100** to the VCSEL structure **200**. First connector portion **304** is used to electrically connect base conductive line **102b** to the fourth conductive layer **218**. In some embodiments, the first connector portion **304** includes more than one conductive portion. In some embodiments, first connector portion **304** is in a two-dimensional plane. In some embodiments, first connector portion **304** is a three-dimensional structure. In some embodiments, the three-dimensional structure includes a combination of conductive lines on different layers. In some embodiments, the first connector portion **304** includes conductive materials including copper, aluminum, nickel, tungsten, titanium, or another suitable conductive material. In some embodiments, the first connector portion **304** includes a soldering material.

Second connector portion **306** is over third conductive layer **214** and is used to connect the EOM structure **100** to the VCSEL structure **200**. Second connector portion **306** is used to electrically connect base conductive line **102a** to the third conductive layer **214**. In some embodiments, the second connector portion **306** includes more than one conductive portion. In some embodiments, second connector portion **306** is in a two-dimensional plane. In some embodiments, second connector portion **306** is a three-dimensional structure. In some embodiments, the three-dimensional structure includes a combination of conductive lines on different layers. In some

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embodiments, the second connector portion **306** includes conductive materials including copper, aluminum, nickel, tungsten, titanium, or another suitable conductive material. In some embodiments, the second connector portion **306** includes a soldering material.

Insulating region **302** is over VCSEL structure **200**. Insulating region **302** is over second passivation region **210**. Insulating region **302** is at least partially over third conductive layer **214** or fourth conductive layer **218**. Insulating region **302** is below EOM structure **100**. Insulating region **302** is below ARC region **108**. Insulating region **302** is at least partially below base conductive line **102a** and base conductive line **102b**. Insulating region **302** at least partially fills where the first opening **104** is shown in the embodiment of FIG. 1 (shown as insulating region **302a** in FIG. 3). Insulating region **302** at least partially fills where the third opening **220** is shown in the embodiment of FIG. 2 (shown as insulating region **302b** in FIG. 3). In some embodiments, insulating region **302** partially fills the region between EOM structure **100** and VCSEL structure **200**. In some embodiments, the insulating region **302** includes a dielectric material with a high refractive index including SiNx; any other suitable material; or combinations thereof. In some embodiments, the insulating region **302** includes a dielectric material with a low refractive index including SiO₂; low-k dielectric; any other suitable material; or combinations thereof. In some embodiments, the insulating region **302** is formed by CVD, spin-on polymeric dielectric or other processes. In some embodiments, the thickness of the insulating region **302** ranges from about 3 μm to about 10 μm . In some embodiments, the insulating region **302** includes one or more layers. In some embodiments, the insulating region **302** is a transparent material. In some embodiments, the insulating region **302** is a same material as the second passivation region **210**. In some embodiments, the insulating region **302** is a different material as the second passivation region **210**.

In some embodiments, EOM/VCSEL structure **300** is a resonant modulator which operates with lower input power when compared with conventional high-bias current VCSEL. In some embodiments, EOM/VCSEL structure **300** is an integrated EOM-VCSEL device with lower operating powers resulting in improved yield and device lifetime. In some embodiments, EOM/VCSEL structure **300** is an integrated EOM-VCSEL device which is directly integrated with electronic circuits. In some embodiments, EOM/VCSEL structure **300** is an integrated EOM-VCSEL device with improved control of the ARC layers **108a**, **108b** and **108c**. In some embodiments, EOM/VCSEL structure **300** is an integrated EOM-VCSEL device with improved control of the first upper reflecting layers **120a**, **120b**, **120c** and **120d**. In some embodiments, EOM/VCSEL structure **300** is configured to operate with a bandwidth of about 50 Gigahertz (GHz). In some embodiments, EOM/VCSEL structure **300** is configured to output an infrared modulated signal with a waist of about 20 μm or less. In some embodiments, EOM/VCSEL structure **300** is configured to output an infrared signal for use in a single-mode optical fiber. In some embodiments, EOM/VCSEL structure **300** is configured to output an infrared signal for use in a multi-mode optical fiber. In some embodiments, EOM/VCSEL structure **300** is configured to output an infrared modulated signal with a wavelength ranging from about 925 nm to about 2000 nm. In some embodiments, the EOM/VCSEL structure **300** is usable for optical communications. In some embodiments, EOM/VCSEL structure **300** is configured to output a modulated signal to contain data. In some embodiments, EOM/VCSEL structure **300** is configured to output a modulated signal that is tunable. In some embodi-

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ments, EOM/VCSEL structure **300** is configured to output an amplitude modulated signal. In some embodiments, EOM/VCSEL structure **300** is configured to output a frequency modulated signal. In some embodiments, EOM/VCSEL structure **300** is configured to output a phase modulated signal. In some embodiments, EOM/VCSEL structure **300** is configured to output a polarization modulated signal.

FIG. 4 is a flow chart of a method **400** of making a VCSEL/EOM structure in accordance with one or more embodiments. Method **400** begins with operation **402** in which a first reflecting region, e.g., first lower reflecting region **204** (FIG. 2), is formed over a first substrate, e.g., first substrate **202** (FIG. 2). In some embodiments, the first reflecting region is formed using CVD, ALD, or other suitable formation processes.

Method **400** continues with operation **404** in which an active semiconductor region, e.g., active semiconductor region **206** (FIG. 2), is formed over the first reflecting region, e.g., first lower reflecting region **204** (FIG. 2). In some embodiments, the active semiconductor region is formed using a deposition process, e.g., metalorganic chemical vapour deposition (MOCVD), Molecular Beam Epitaxy (MBE), or other suitable formation processes.

Method **400** continues with operation **406** in which a second reflecting region, e.g., second upper reflecting region **208** (FIG. 2), is formed over an active semiconductor region, e.g., active semiconductor region **206** (FIG. 2). In some embodiments, the second reflecting region is formed using CVD, ALD, or other suitable formation processes.

Method **400** continues with operation **408** in which a passivation region, e.g., passivation region **210** (FIG. 2), is formed over the first reflecting region, e.g., first lower reflecting region **204** (FIG. 2), second reflecting region, e.g., second upper reflecting region **208** (FIG. 2), or the active semiconductor region, e.g., active semiconductor region **206** (FIG. 2). In some embodiments, the passivation region is formed using CVD, spin-on polymeric dielectric or other suitable formation processes.

Method **400** continues with operation **410** in which at least one conductive line, e.g., third conductive line **212** (FIG. 2) or fourth conductive line **216** (FIG. 2), is formed in the passivation region, e.g., second passivation region **210** (FIG. 2). In some embodiments, the conductive line is formed using a combination of photolithography and material removal processes to form openings in the passivation region. In some embodiments, the photolithography process includes patterning a photoresist, such as a positive photoresist or a negative photoresist. In some embodiments, the photolithography process includes forming a hard mask, an antireflective structure, or another suitable photolithography structure. In some embodiments, the material removal process includes a wet etching process, a dry etching process, an RIE process, laser drilling or another suitable etching process. The openings are then filled with conductive material, e.g., copper, aluminum, titanium, nickel, tungsten, or other suitable conductive material. In some embodiments, the openings are filled using CVD, PVD, sputtering, ALD or other suitable formation process.

Method **400** continues with operation **412** in which at least one P- or N-doped region, e.g., first doped region **110** or second doped region **118**, is formed in a modulation region, e.g., a modulation region **112** (FIG. 1). In some embodiments, at least one P- or N-doped region is doped with dopants suitable for Silicon, Silicon/Germanium and Germanium. In some embodiments, the P- or N-doped regions formed using implantation, diffusion or other suitable formation processes.

Method **400** continues with operation **414** in which a third reflecting region, e.g., first upper reflecting region **120** (FIG.

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1), is formed over modulation region, e.g., modulation region **112** (FIG. 1). In some embodiments, the third reflecting region is formed over the modulation region by backside illuminated processes, KOH backside etch processes with an implantation etch stop, CVD, ALD, or other suitable formation processes.

Method **400** continues with operation **416** in which at least one conductive line, e.g., first conductive line **114** (FIG. 1) or second conductive line **124** (FIG. 1), is formed in the modulation region, e.g. modulation region **112** (FIG. 1). In some embodiments, the conductive line is formed using a combination of photolithography and material removal processes to form openings in the modulation region. In some embodiments, the photolithography process includes patterning a photoresist, such as a positive photoresist or a negative photoresist. In some embodiments, the photolithography process includes forming a hard mask, an antireflective structure, or another suitable photolithography structure. In some embodiments, the material removal process includes a wet etching process, a dry etching process, an RIE process, laser drilling or another suitable etching process. The openings are then filled with conductive material, e.g., copper, aluminum, titanium, nickel, tungsten, or other suitable conductive material. In some embodiments, the openings are filled using CVD, PVD, sputtering, ALD or other suitable formation process.

Method **400** continues with operation **418** in which an Anti-Reflection Coating, e.g., ARC region **108** (FIG. 1), is formed over an opposite side of modulation region, e.g., modulation region **112** (FIG. 1). In some embodiments, the Anti-Reflection Coating is formed using CVD, ALD, PVD, or other suitable formation processes.

Method **400** continues with operation **420** in which at least one conductive layer, e.g., base conductive line **102a** (FIG. 1) or base conductive line **102b** (FIG. 1), is formed in the Anti-Reflection Coating, e.g. ARC region **108** (FIG. 1). In some embodiments, the conductive layer is formed using a combination of photolithography and material removal processes to form openings in the Anti-Reflection Coating. In some embodiments, the photolithography process includes patterning a photoresist, such as a positive photoresist or a negative photoresist. In some embodiments, the photolithography process includes forming a hard mask, an antireflective structure, or another suitable photolithography structure. In some embodiments, the material removal process includes a wet etching process, a dry etching process, an RIE process, laser drilling or another suitable etching process. The openings are then filled with conductive material, e.g., copper, aluminum, titanium, nickel, tungsten, or other suitable conductive material. In some embodiments, the openings are filled using CVD, PVD, sputtering, ALD or other suitable formation process.

Method **400** continues with operation **420** in which the EOM structure, e.g. EOM structure **100** (FIG. 1), is connected to the VCSEL structure, e.g., VCSEL structure **200** (FIG. 2). In some embodiments, the EOM structure is connected to the VCSEL structure using a laser bonding process, a conductive adhesive layer, a soldering bump process or another suitable bonding process.

One of ordinary skill in the art would recognize that an order of operations in method **400** is adjustable. One of ordinary skill in the art would further recognize that additional steps are able to be included in method **400** without departing from the scope of this description.

One aspect of this description relates to an electro-optic modulator including a semiconductor region, a first reflecting region over the semiconductor region and an anti-reflecting region on an opposite surface of the semiconductor region

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from the first reflecting layer. The semiconductor region includes a first doped region and a second doped region.

Another aspect of this description relates to an integrated electro-optic modulator/laser comprising a substrate, a first reflecting region over the substrate, a first semiconductor region over the first reflecting region, a second reflecting region over the first semiconductor region, an anti-reflecting region over the second reflecting layer, a second semiconductor region over the anti-reflecting layer and a third reflecting region over the second semiconductor region. The second semiconductor region comprises a first doped region and a second doped region.

Still another aspect of this description relates to a method of making an electro-optic modulator, the method comprises forming at least one of a first doped region or a second doped region in a modulation region, forming a first reflecting region on the modulation region and forming an anti-reflection coating on the modulation region.

It will be readily seen by one of ordinary skill in the art that the disclosed embodiments fulfill one or more of the advantages set forth above. After reading the foregoing specification, one of ordinary skill will be able to affect various changes, substitutions of equivalents and various other embodiments as broadly disclosed herein. It is therefore intended that the protection granted hereon be limited only by the definition contained in the appended claims and equivalents thereof.

What is claimed is:

1. An electro-optic modulator device comprising: a semiconductor region, wherein the semiconductor region comprises: a first doped region; and a second doped region; a first reflecting region over the semiconductor region; a first conductive line electrically connected to the first doped region or the second doped region, wherein the first conductive line extends through the first reflecting region; and an anti-reflecting region on an opposite surface of the semiconductor region from the first reflecting layer.
2. The electro-optic modulator of claim 1, wherein the first doped region comprises one of a P-doped region or an N-doped region.
3. The electro-optic modulator of claim 1, wherein the second doped region comprises one of a P-doped region or an N-doped region.
4. The electro-optic modulator of claim 1, further comprising: a first opening, wherein the first opening is configured to receive an infrared radiation; and a second opening, wherein the second opening is configured to send a modulated output radiation.
5. The electro-optic modulator of claim 4, wherein the modulated output is amplitude modulated, frequency modulated, phase modulated or polarization modulated.
6. The electro-optic modulator of claim 1, wherein the first doped region is adjacent to a lower portion of the semiconductor region.
7. The electro-optic modulator of claim 1, wherein the second doped region is adjacent to an upper portion of the semiconductor region.
8. The electro-optic modulator of claim 1, wherein the semiconductor region comprises Si, Ge or SiGe.
9. The electro-optic modulator of claim 1, wherein the semiconductor region comprises at least one quantum well.

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10. The electro-optic modulator of claim 9, wherein the at least one quantum well comprises Si, Ge or SiGe.

11. The electro-optic modulator of claim 9, wherein the at least one quantum well comprises a number of quantum well layers ranging from about 1 layer to about 31 layers.

12. An integrated electro-optic modulator/laser device comprising:

- a substrate;
- a first reflecting region over the substrate;
- a first semiconductor region over the first reflecting region;
- a second reflecting region over the first semiconductor region;
- an anti-reflecting region over the second reflecting region;
- a second semiconductor region over the anti-reflecting region, wherein the second semiconductor region comprises a first doped region and a second doped region; and
- a third reflecting region over the second semiconductor region.

13. The electro-optic modulator/laser of claim 12, wherein the second semiconductor region comprises a thickness of the second semiconductor region ranging from about 2 microns (μm) or less.

14. The electro-optic modulator/laser of claim 12, wherein the third reflecting region comprises a distributed bragg reflector.

15. The electro-optic modulator/laser of claim 12, wherein the third reflecting region comprises a number of reflecting layers ranging from about 10 layers to about 20 layers.

16. The electro-optic modulator/laser of claim 12, wherein the anti-reflecting region comprises a number of anti-reflecting layers ranging from about 3 layers to about 10 layers.

17. The electro-optic modulator of claim 12, further comprising:

- a distance between a top surface of a second reflecting region and a top surface of a second semiconductor region, wherein the distance ranges from about 25 μm or less.

18. A method of making an electro-optic modulator device, the method comprising:

- forming at least one of a first doped region or a second doped region in a modulation region;
- forming a first reflecting region on the modulation region;
- forming a first conductive line in the modulation region electrically connecting the first doped region or the second doped region, the first conductive line extends through the first reflecting region; and
- forming an anti-reflection coating on the modulation region.

19. The method of claim 18, further comprising: forming a metal layer on the anti-reflection coating.

- 20. The method of claim 19, further comprising: forming a second reflecting region over a substrate;
- forming a semiconductor region over the second reflecting region;
- forming a third reflecting region over the semiconductor region;
- forming a passivation region on at least one of the second reflecting region, the third reflecting region or the semiconductor region;
- forming a second conductive line in the passivation region electrically connecting the second conductive line to the second reflecting region or the third reflecting region; and
- connecting the second conductive line to the metal layer.

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